A 1.4mA & 3mW, SiGe90, BiFET Low Noise Amplifier for Wireless Portable Applications

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Abstract — **A 3 mW silicon-based LNA has been built using a novel cascoded Bipolar/mosFET (BiFET) configuration in SiGe90, a SiGe BiCMOS process optimized for next-generation wireless applications. Ultra-low current (1.4mA) and power consumption (3mW) is achieved with a 16dB power gain, a 1.6dB minimum noise figure and –6.5dBm IIP3 operating in the PCS band. By using this cascoded configuration, the BiFET LNA can operate up to 5V and reach a high power gain of over 20dB. This LNA has been packaged and measured through an input & output 50ohm PC board match. To the best of our knowledge, this is the lowest current silicon-based LNA reported to date which maintains good PCS band performance.**

I. INTRODUCTION

Wireless portable communications have become increasingly popular in daily activities. The battery life in portable communication systems is largely determined by the circuit power consumption. This is especially true for the receiver LNA since it must be continuously powered to explore the pilot signal. At the same time, the LNA has to provide a high gain, linearity and low noise figure to maintain good receiver system specifications.

To satisfy the low current and low power requirement, III-V PHEMT process technology was used previously to achieve a record LNA of 1.7mA and 5mW at 2.4GHz band [1]. Recently, SiGe90, a SiGe BiCMOS process technology optimized for wireless applications has been reported [2,3] and used to fabricate a PCS LNA with a record sub-1dB noise figure and nearly equal low-power performance at 2.75 mA and ~8 mW [4].

In this paper, we report on the combination of SiGe90 with a novel cascoded **Bi**polar/mos**FET (BiFET)** design, which achieves an even lower power consumption of only 3 mW operating at a current of 1.4 mA while maintaining good gain, linearity and noise performance in the PCS band. To our knowledge, this is the lowest power PCS-band LNA reported to date.

II. THE BIFET LNA CONFIGURATION

Today a variety of LNA configurations are in use. Single device LNAs as shown in Figure 1 generally have lower power gain than cascaded LNAs shown in Figure 2 but consume less power. The cascoded LNA shown in Figure 3(a) and 3(b) has been used to maintain low power consumption and higher gain simultaneously. Implementations that use only bipolar devices typically have better noise figure while implementations that use MOS devices can achieve higher linearity. This is due to the inherent properties of the bipolar and MOS device. In this paper, we propose a cascoded **Bi**polar/mos**FET (BiFET)** configuration as shown in Figure 3(c). Such an approach combines a very low-noise bipolar first stage with a linear cascoded MOSFET (BiFET) to improve the tradeoff between power consumption, noise, gain and linearity relative to the more traditional configurations shown in Figures 1 through 3(b).

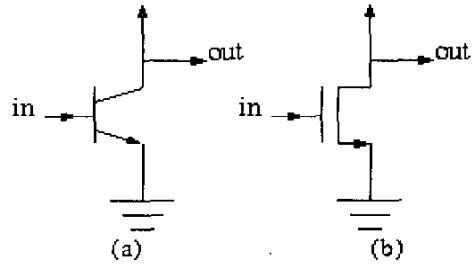

Fig.1. Single-device LNA with a Bipolar (a) and MOSFET (b) configuration, respectively.

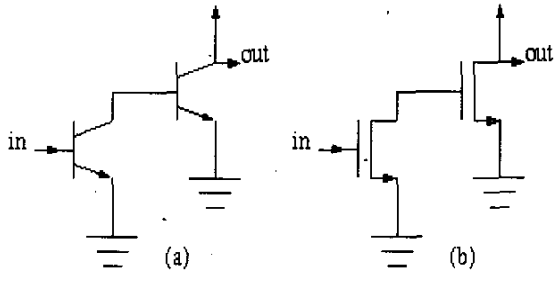

Fig.2. Cascaded LNA with a Bipolar (a) and MOSFET (b) configuration, respectively.

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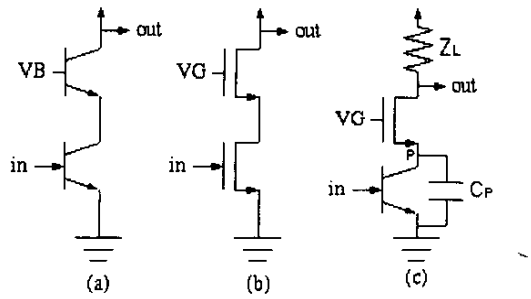


Fig.3. Cascoded LNA with a Bipolar (a), MOSFET (b) and BiFET (c) configuration, respectively.

Some analysis of the configuration shown in Figure 3(c) follows. In this configuration, the Bipolar is cascoded with a MOSFET loading an impedance Z_L. The capacitance at node P is marked as C_P for further analysis. Using the small-signal frequency response, we can obtain a voltage gain as [5]:

$$V_{out}/V_{in}(s)=-g_{mBip}Z_L\cdot g_{mMOS}/(g_{mMOS}+C_Ps) \quad (1)$$

Where g_{mBip} and g_{mMOS} is the Bipolar and MOSFET transconductance respectively. For a lower operating frequency, $g_{mMOS}>>C_Ps$, Eq.(1) can be reduced to

$$V_{out}/V_{in}(s)=-g_{mBip}Z_L \quad (2a)$$

The LNA operates in a cascoded mode. For a higher operational frequency, $g_{mMOS}<<C_Ps$, Eq.(1) can be reduced to

$$V_{out}/V_{in}(s)=(-g_{mBip}\cdot 1/C_Ps)\cdot(g_{mMOS}\cdot Z_L)$$

$$=A_{Bip}\cdot A_{MOS} \quad (2b)$$

Where A_{Bip} and A_{MOS} is the voltage gain for the Bipolar and MOSFET stage respectively. In this case, the LNA operates in a cascaded mode. In the actual application band, the LNA operates between the cascoded and cascaded modes of operation.

For DC operation, the BiFET LNA can operate at nearly the same current as a singe-device LNA. For RF operation, we can consider the BiFET LNA when operating in two extreme cases, the cacoded and cascaded mode. In the cacoded mode, the BiFET LNA has equivalent noise figure, linearity and power consumption as the bipolar single-device LNA (Fig.1(a)) but with a higher gain. In the cascaded mode, the BiFET LNA has a noise figure that is mainly determined by the bipolar stage while linearity that is mainly determined by the MOSFET stage while still consuming the same power as a single stage LNA. Thus one can achieve a better tradeoff between noise, linearity, gain, and power consumption than is possible with other, more traditional configurations. To make this configuration possible, both a high performance (low noise) bipolar device, and together with an advanced geometry MOS device is required as offered in SiGe90 [2,3].

III. Design and Fabrication

The BiFET LNA is designed using the Jazz 0.18um SiGe90 process. This technology offers two types of SiGe NPNs: a 75GHz Ft, 130GHz Fmax, 3.8V BVceo high speed device and a 35GHz Ft, 100GHz Fmax, 6V BVceo high voltage device. It also offers poly resistors, 3.3 V CMOS, high-Q MIM capacitors, and high-Q inductors. This process used includes a 4 um thick top metal inductor built on an 8 ohm-cm silicon substrate. More details on the technology can be found in the references [2,3].

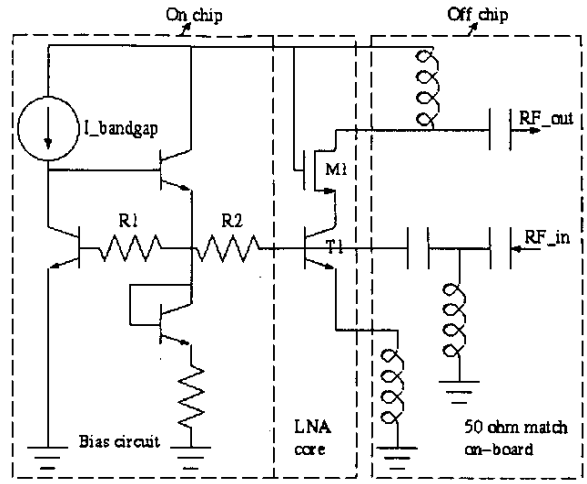


Fig.4. The simplified LNA schematic design.

The BiFET LNA includes the LNA core, bandgap-referenced circuit and input & output 50ohm on-board match. In the Fig.4, The bipolar transistor T1 has been optimally sized to match the MOSFET M1 for best RF performance. The bias circuit provides a direct bandgap-referenced current to bias the LNA core through a current mirror. The input and output are matched to 50 ohm by using on-board inductors and capacitors.

The fabricated LNA is packaged in a 32 pin LGA. As shown in Fig.5, four versions of the LNA are designed in each corner of the package to explore the performance space. An LNA (center of the die) is also designed to be on-wafer testable.

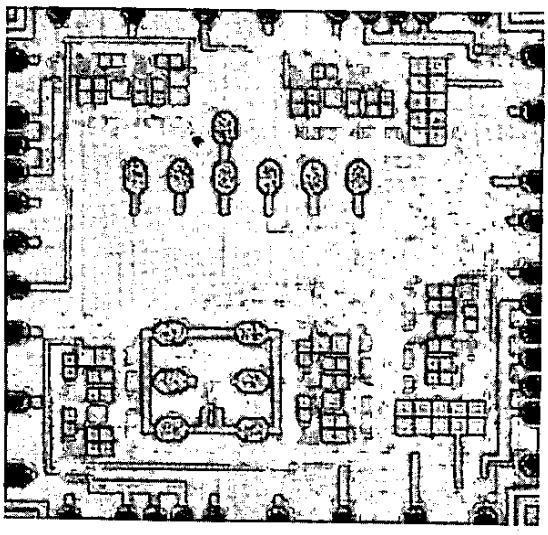


Fig.5. The BiFET LNA as fabricated. Where four versions of the LNA are fabricated in the each corner of die and the on-chip test version is located in the center of the die.

VI. TEST RESULT

The fabricated LNA is measured at room temperature with a supply voltage ranging from 2.2V to 5V. As Fig.6 shows, the LNA achieves a 16dB power gain, -6.5dBm IIP3 and 1.43mA/3.1mW power consumption at 2.2V supply voltage. Above 2.4 V, the power gain exceeds 19 dB and remains in the 19~20 dB range up to a supply of 5 V. The current also remains a 3mA level up to the 5 V supply.

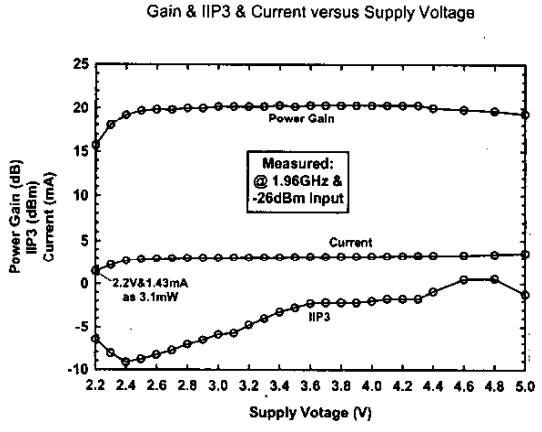
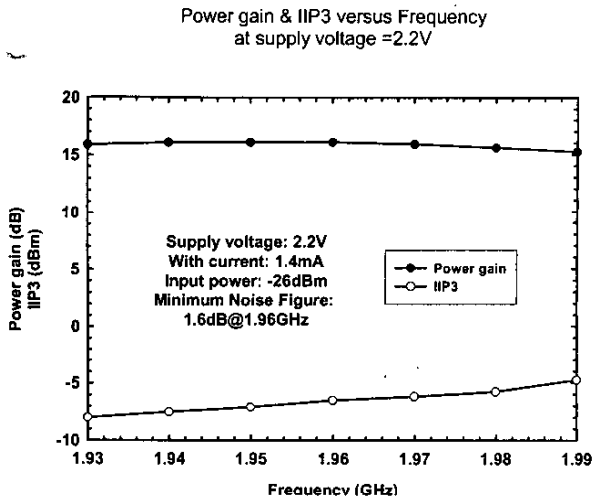
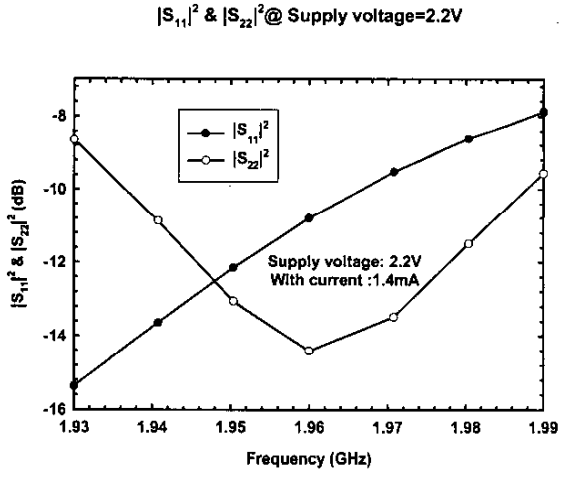


Fig.6 Power gain, IIP3 and current consumption versus supply voltage.

The RF performance versus operating frequency is measured at 2.2V, 3.0V and 5.0V and the result is plotted in Fig.7, Fig.8 and Fig.9, respectively. The power gain, noise figure, and IIP3 exhibit a smooth variation with the operating frequency. A typical result at 1.96GHz is marked in each figure.

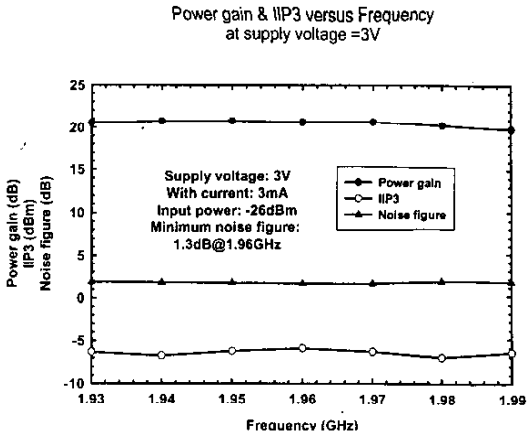


(a)

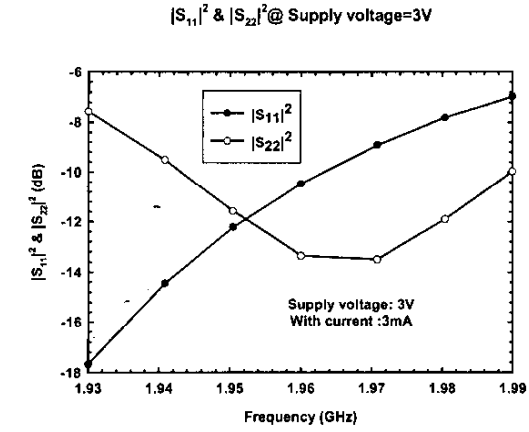


(b)

Fig.7 The power gain & IIP3 (a) and input & output return loss (b) versus frequency at 2.2V.



(a)



(b)

Fig.8 The power gain & IIP3 & noise figure (a) and input & output return loss (b) versus frequency at 3.0V.

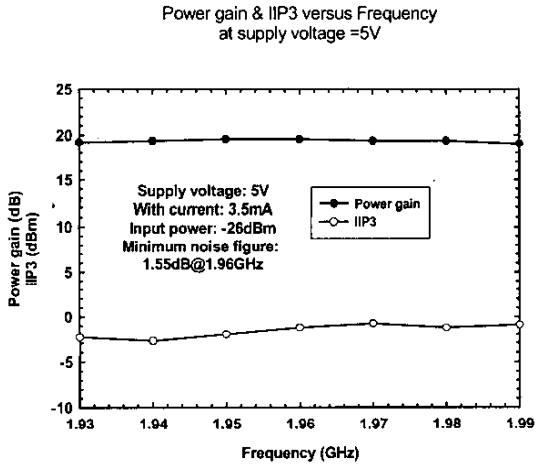


Fig.9. The power gain & IIP3 versus frequency at 5V.

V. Conclusion

In this paper, we have utilized Jazz's SiGe90 BiCMOS process technology to realize a novel LNA configuration named the BiFET LNA. This LNA merges the low noise advantage of SiGe bipolar devices with the inherent linearity advantages of MOSFET devices together with the low current and high gain advantage of a cascode configuration to improve the power consumption, gain, noise and linearity tradeoff in LNA design. The LNA has been built, packaged and tested. It consumes only 3mW while achieving a PCS-band gain of 16dB, a noise figure of 1.6dB and IIP3 of -6.5dBm. The LNA is operational at a supply voltage of 2.2 to 5 V and achieves a power gain of 19 dB with a supply of only 2.4 V. To our knowledge this is the lowest power consumption reported for an LNA capable of meeting PCS-band requirements.

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